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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,602	09/08/2003	Hans Taddiken	P2001,0166	1770

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EXAMINER	
PARK, JOHN J	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,602	TADDIKEN, HANS	
	Examiner	Art Unit	
	John J. Park	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *herewith*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as anticipated by Campbell et al. (U.S. patent No. 5,844,416).

Re claim 1, a circuit for detecting a focused ion beam attack (Fig.1; Col.3 Line45-47; Col.4 Line18-26), comprising:

a memory cell; (Col.8 Line13-17; Col.9 Line46-Col.10 Line19)

an antenna for detecting an FIB attack connected to said memory cell; (Fig.2A; Col.6 Line33-46; Col.7 Line47-Col.8 Line17)

a driver circuit; (Fig.1; Col.3 Line38-45) and

a capacitance connected between said memory cell and said driver circuit, for isolating said driver circuit from said antenna. (Col.5 Line30-Col.6 Line15)

Re claim 4, the circuit according to claim 1, wherein said memory cell is one of two memory cells connected to said antenna and isolated from said driver circuit by said capacitance. (Col.4 Line54-56; Col.5 Line30-Col.6 Line15)

Therefore, Campbell et al. reasonably can be read to describe every limitation of claims 1 and 4.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. patent No. 5,844,416) in view of Hosono et al. (U.S. patent No. 6,404,274).

Re claim 2, Campbell et al. disclose a focused ion beam (FIB) apparatus and method for controlling integrated circuits. (Col.2 Line30-34) The apparatus comprises one or more ICs (Col.3 Line38-45), a source means for producing a FIB, and a beam-directing means for directing the FIB to irradiate a predetermined location of the IC for a period of time to provide an incident ion-beam-generated electrical input signal to predetermined element of the IC (Col.4 Line54-56) that is the surface of a gate of a transistor or an electrically conducting material to a transistor, capacitor (Col.5 Line30-43), resistor, or memory cell (Col.9 Line46-Col.10 Line8). A circuit diagram and a unit memory cell of an integrated circuit are analyzed and controlled with an ion-beam apparatus and method. (Col.10 Line5-9) A secondary particle detector, a microchannel plate detector, and an electron floodgun above IC further allow a partial removal or erasure of the ion-beam-generated electrical input signal. (Col.6 Line33-46)

However, Campbell et al. fail to teach a memory cell selected from the group consisting of a floating gate cell, an EEPROM cell, a flash cell, and a SONOS cell.

Hosono et al. disclose an integrated circuit incorporating an electrically programmable and erasable nonvolatile memory cell, e.g., an EEPROM or flash memory in which a floating gate and a control gate are stacked. (Col.2 Line65-Col.3 Line14)

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the EEPROM or flash memory as a nonvolatile memory cell as taught by Hosono et al. into the teachings of Campbell et al. in order to stack the nonvolatile memory on a semiconductor substrate for memory to allow high integration and batch erase operation.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Campbell et al. (U.S. patent No. 5,844,416) in view of Yamazaki (U.S. patent No. 6,686,623).

Re claim 3, the teachings of Campbell et al. have been discussed above.

However, Campbell et al. fail to teach an electrically conductive electrode over a silicon area in memory cells.

Yamazaki discloses circuits configured by using nonvolatile memory cells having multi-layer electrode structure over a silicon substrate for nonvolatile memory cells. (Col.10 Line9-25; Col.16 Line55-60)

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to employ the electrode structure in a silicon substrate as taught by Yamazaki into the teachings of Campbell et al. in order to apply the electrode structure which is

directed to a memory cell having a basic stacked structure that would efficiently extract holes generated by impact ionization.

Allowable Subject Matter

6. The following is a statement of reasons for the indication of allowable subject matter:

The ~~closest~~ prior art of the record do not disclose, teach, or fairly suggest that a circuit connects for operation as a FIB sensor of a smart card IC.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Itoh et al. (U.S. patent No. 5,656,811) disclose a method for making a specimen for use in observation through a transparent electron microscope which can be observed through a transparent electron microscope by scanning and irradiating a FIB onto the specimen; Iwamoto et al. (U.S. patent No. 5,434,422) disclose a sample position controller in a FIB system in which a reference unit quantity on a surface of a sample is calculated on the basis of the quantity of movement of the sample.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Park whose telephone number is 571-272-2350. The examiner can normally be reached on 5:30am - 2:00pm (Monday - Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on 571-272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J Park
Examiner
Art Unit 2876

STEVEN PARK
PRIMARY EXAMINER